

CLAIMS

What is claimed is:

1. An imager cell comprising:
 - 5 a photoreceptor;
 - a sense node; and
 - a pinned transfer gate disposed to transfer charge between the photoreceptor and the sense node.
2. An imager cell as defined in claim 1, wherein the pinned transfer gate comprises a p-doped pinned region in an n-doped transfer region.
3. An imager cell as defined in claim 1, further comprising a photoreceptor readout gate disposed above the photoreceptor.
4. An imager cell as defined in claim 1, wherein the photoreceptor comprises a photogate.
- 15 5. An imager cell as defined in claim 1, wherein the photoreceptor comprises a photodiode.
6. An imager cell as defined in claim 1, further comprising a reset transistor disposed to reset the sense node.
7. An imager cell as defined in claim 1, further comprising an output amplifier coupled 20 to the sense node.
8. An imager cell as defined in claim 7, wherein the output amplifier is a source follower amplifier.
9. An imager cell as defined in claim 3, further comprising a readout clock connection coupled to the photoreceptor readout gate.

10. An imager cell as defined in claim 9, further comprising control circuitry coupled to the readout clock connection, the control circuitry supplying a photoreceptor readout clock.

11. An imager cell as defined in claim 10, wherein the photoreceptor readout clock is characterized by a V+ level applied during an integration period, and a V- level applied
5 during a transfer period.

12. An imager cell comprising:

13. a photoreceptor;

14. a sense node;

15. a pinned transfer gate disposed to transfer charge between the photoreceptor and the sense node; and

16. a photoreceptor readout gate disposed above the photoreceptor, the photoreceptor readout gate having material removed to form a photoreceptor readout gate light aperture above the photoreceptor, whereby the photoreceptor provides enhanced response to blue light.

17. An imager cell as defined in claim 12, further comprising a pinned aperture region under the photoreceptor readout gate light aperture.

18. An imager cell as defined in claim 12, wherein the pinned transfer gate comprises a p-doped pinned region in an n-doped transfer region.

19. An imager cell as defined in claim 12, wherein the photoreceptor comprises a
20. photogate.

21. An imager cell as defined in claim 12, wherein the photoreceptor comprises a photodiode.

22. An imager cell as defined in claim 12, further comprising a reset transistor disposed to reset the sense node.

18. An imager cell as defined in claim 12, further comprising an output amplifier coupled to the sense node.

19. An imager cell as defined in claim 18, further comprising an anti-reflective coating disposed above the photoreceptor.

5 20. An imager cell as defined in claim 12, further comprising a readout clock connection coupled to the photoreceptor readout gate.

14 21. An imager cell as defined in claim 20, further comprising control circuitry coupled to the readout clock connection, the control circuitry supplying a photoreceptor readout clock.

15 22. An imager cell as defined in claim 21, wherein the photoreceptor readout clock is characterized by a V+ level applied during an integration period, and a V- level applied during a transfer period.

23. An imager cell comprising:

16 a photoreceptor;

17 a sense node;

18 a pinned transfer gate disposed to transfer charge between the photoreceptor and the sense node; and

19 a photoreceptor readout gate disposed above the photoreceptor, the photoreceptor readout gate characterized by a photoreceptor readout gate thickness of less than 2000 Angstroms, whereby the photoreceptor provides enhanced response to blue light.

20 24. An imager cell as defined in claim 23, wherein the photoreceptor readout gate thickness is less than 1000 Angstroms.

25. An imager cell as defined in claim 23, wherein the photoreceptor readout gate thickness is less than 500 Angstroms.

26. An imager cell as defined in claim 23, wherein the pinned transfer gate comprises a p-doped pinned region in an n-doped transfer region.

27. An imager cell as defined in claim 23, wherein the photoreceptor comprises a photogate.

28. An imager cell as defined in claim 23, wherein the photoreceptor comprises a photodiode.

5 29. An imager cell as defined in claim 23, further comprising a reset transistor disposed to reset the sense node.

10 30. An imager cell as defined in claim 23, further comprising an output amplifier coupled to the sense node.

15 31. An imager cell as defined in claim 28, wherein the output amplifier is a source follower amplifier.

32. An imager cell as defined in claim 23, further comprising a readout clock connection coupled to the photoreceptor readout gate.

33. An imager cell as defined in claim 32, further comprising control circuitry coupled to the readout clock connection, the control circuitry supplying a photoreceptor readout clock.

15 34. An imager cell as defined in claim 33, wherein the photoreceptor readout clock is characterized by a V+ level applied during an integration period, and a V- level applied during a transfer period.

20 35. ~~A method of manufacturing an imager cell, the method comprising:~~
~~fabricating a photoreceptor in a semiconductor substrate;~~
~~fabricating a sense node in the substrate; and~~
~~fabricating a pinned transfer gate in the substrate disposed to transfer charge between~~
~~the photoreceptor and the sense node.~~

25 36. A method as defined in claim 35, wherein ~~fabricating the pinned transfer gate~~ comprises fabricating an n-doped transfer region and fabricating a p-doped pinned region in the n-doped transfer region.

14 37. A method as defined in claim 35, further comprising fabricating a photoreceptor
readout gate disposed above the photoreceptor.

15 38. A method as defined in claim 35, wherein fabricating a photoreceptor comprises
fabricating a photogate.

5 39. A method as defined in claim 35, wherein fabricating a photoreceptor comprises
fabricating a photodiode.

10 40. A method as defined in claim 35, further comprising fabricating a reset transistor
disposed to reset the sense node.

11 41. A method as defined in claim 35, further comprising fabricating an output amplifier
coupled to the sense node.

12 42. A method as defined in claim 41, wherein fabricating an output amplifier comprises
fabricating a source follower amplifier.

13 43. A method of manufacturing an imager cell, the method comprising:
14 fabricating a photoreceptor in a semiconductor substrate;

15 fabricating a sense node in the substrate; and
16 fabricating a pinned transfer gate in the substrate disposed to transfer charge between
17 the photoreceptor and the sense node; and
18 fabricating a photoreceptor readout gate disposed above the photoreceptor, the
19 photoreceptor readout gate having material removed to form a photoreceptor readout gate
20 light aperture above the photoreceptor.

21 44. A method as defined in claim 43, further comprising fabricating a pinned aperture
region under the photoreceptor readout gate light aperture.

22 45. A method as defined in claim 43, wherein fabricating the pinned transfer gate
comprises fabricating an n-doped transfer region and fabricating a p-doped pinned region in
23 the n-doped transfer region.

46. A method as defined in claim 43, wherein fabricating a photoreceptor comprises fabricating a photogate.

47. A method as defined in claim 43, wherein fabricating a photoreceptor comprises fabricating a photodiode.

5 48. A method as defined in claim 43, further comprising fabricating a reset transistor disposed to reset the sense node.

49. A method as defined in claim 43, further comprising fabricating an output amplifier coupled to the sense node.

50. A method as defined in claim 49, wherein fabricating an output amplifier comprises fabricating a source follower amplifier.

51. A method of manufacturing an imager cell, the method comprising:
fabricating a photoreceptor in a semiconductor substrate;
fabricating a sense node in the substrate; and
fabricating a pinned transfer gate in the substrate disposed to transfer charge between
15 the photoreceptor and the sense node; and
fabricating, above the photoreceptor, a photoreceptor readout gate of a thickness less
than 2000 Angstroms.

52. An method as defined in claim 51, wherein fabricating the pinned transfer gate comprises fabricating an n-doped transfer region and fabricating a p-doped pinned region in
20 the n-doped transfer region.

53. An method as defined in claim 51, wherein fabricating a photoreceptor comprises fabricating a photogate.

54. An method as defined in claim 51, wherein fabricating a photoreceptor comprises fabricating a photodiode.

55. An method as defined in claim 51, further comprising fabricating a reset transistor disposed to reset the sense node.

56. An method as defined in claim 51, further comprising fabricating an output amplifier coupled to the sense node. *A*

5 57. An method as defined in claim 57, wherein fabricating an output amplifier comprises fabricating a source follower amplifier.

58. An imager cell comprising:
means for detecting incident photons;
means for storing transferred charge for readout; and
a pinned transfer gate disposed to transfer charge between the means for detecting and the means for storing.

59. An imager cell as defined in claim 58, wherein the pinned transfer gate comprises a p-doped pinned region in an n-doped transfer region.

60. An imager cell as defined in claim 58, further comprising means for transferring charge from the means for detecting incident photons to the pinned transfer gate.

15 61. An imager cell as defined in claim 58, further comprising means for resetting the means for storing transferred charge.

62. An imager cell as defined in claim 58, further comprising means for amplifying the transferred charge.

20 63. An imager cell as defined in claim 60, further comprising means for clocking the means for transferring charge.

64. An imager cell as defined in claim 63, wherein the means for clocking is characterized by a V+ level applied during an integration period, and a V- level applied during a readout transfer period.

65. An imager cell as defined in claim 60, wherein the means for transferring charge comprises a photoreceptor readout gate characterized by a thickness of less than 2000 Angstroms.

66. An imager cell as defined in claim 61, wherein the means for transferring charge 5 comprises a photoreceptor readout gate characterized by a thickness of less than 1000 Angstroms.

67. An imager cell as defined in claim 61, wherein the means for transferring charge comprises a photoreceptor readout gate characterized by a thickness of less than 500 Angstroms.

68. An imager cell as defined in claim 60, wherein the means for transferring charge comprises a photoreceptor readout gate having material removed to form a photoreceptor readout gate light aperture above the means for detecting incident photons.

69. An imager cell as defined in claim 68, further comprising a pinned aperture region under the photoreceptor readout gate light aperture.

15 70. An imaging array comprising:

an array of imager cells, each imager cell comprising a photoreceptor, a sense node, and a photoreceptor readout gate; and wherein at least one of the imager cells further comprises a pinned transfer gate disposed to transfer charge between the photoreceptor and the sense node; and

20 control circuitry coupled to each photoreceptor readout gate for supplying a photoreceptor readout clock simultaneously to a set of photoreceptors in the array, whereby accumulated charge in each photoreceptor is transferred to its sense node to provide a snapshot of an image acquired by the imaging array.

71. An imager cell comprising:

- a photoreceptor including a photoreceptor readout gate;
- a sense node;
- a pinned transfer gate disposed to transfer charge between the photoreceptor and the
- 5 sense node; and
- control circuitry coupled to the photoreceptor readout gate for applying a photoreceptor readout clock to the photoreceptor readout gate, the photoreceptor readout clock comprising an integration period characterized by an integration voltage selected from a plurality of predetermined integration voltages to setup a preselected charge capacity level in the photoreceptor.

14
13
12
11
10
9
8
7
6
5
4
3
2
1
0